REMARKS

The Office action mailed on 27 March 2003 (Paper No. 24) has been carefully considered.

The specification is being amended to correct minor errors and improve form. Claims 3 and 6 thru 8 are being canceled without prejudice or disclaimer, claims 1, 2, 4, 5, 9 and 10 are being amended, and claims 11 thru 43 are being added. Thus, claims 1, 2, 4, 5 and 9 thru 43 are pending in the application.

In paragraph 2 of the Office action, the Examiner rejected claims 1, 9 and 10 under 35 U.S.C. § 103(a) for alleged unpatentability over Ozolins U.S. Patent No. 5,990,858. In paragraph 4 of the Office action, the Examiner rejected claims 3 thru 8 under 35 U.S.C. § 103(a) for alleged unpatentability over Ozolins '858 in view of Rokunohe *et al.* U.S. Patent No. 4,549,175. In paragraph 6 of the Office action, the Examiner rejected claim 2 under 35 U.S.C. § 103(a) for alleged unpatentability over Ozolins '858 in view of Sawada, U.S. Patent No. 6,078,317. For the reasons stated below, it is submitted that the invention recited in the claims, as now amended, is distinguishable from the prior art cited by the Examiner so as to preclude rejection under 35 U.S.C. §102 or §103.

Ozolins '858 discloses a flat panel display terminal for receiving multi frequency and multi-protocol video signals. As seen in Figure 1, the flat panel display 10 basically comprises an interface 20 connected to an analog liquid crystal display (LCD) panel 30.

In paragraph 3 on page 2 of the Office action, the Examiner states that "Ozolins discloses a flat panel display apparatus for receiving display information including video data (40)" (quoting from paragraph 3, lines 1-2 of the Office action). Actually, contrary to the assertion by the Examiner, element 10 in Figure 1 of Ozolins '858 constitutes a flat panel display apparatus which includes the interface 20 and an analog LCD panel 30.

In paragraph 3 of the Office action, the Examiner proceeds to assert that element 20 is a receiver which "receives input signals originating from the graphic controller and output[s] signals to analog LCD panel (30)" (quoting from paragraph 3, lines 2-3 of the Office action). Actually, cable adaptor 40 of interface 20 in Figure 1 of Ozolins '858 receives various types of video signals from the graphic board of a computer (*see* column 3, lines 10-11 of the patent).

In paragraph 3 of the Office action, the Examiner appears to suggest that the "receiver (20)", phase-locked loop (PLL) circuit board (90), brightness controller (100), and microprocessor (80) are constituent parts of "a flat panel display apparatus for receiving display information including video data (40)" (quoting from paragraph 3 on page 2 of the Office action). However, contrary to this assertion by the Examiner, a review of Figure 1 clearly indicates that element 20, 80, 90 and 100 of Figure 1 of Ozolins '858 are not constituent parts of element 40 thereof. Rather, ~~cable~~ adapter 40, microprocessor 80, PLL circuit 90 and brightness controller 100 are constituent parts of interface 20.

Further considering claim 1 of the present application, as now amended, the Examiner does not identify an element of Ozolins '858 corresponding to the claimed receiver for reconstructing

display information. In that regard, whereas the video cable adapter 40 of Ozolins '858 "receives various types of video signals from the computer's graphic board", and "passes the RGB signal portion of the video signals to analog LCD panel 30" (quoting from column 3, lines 10-13 of the patent), it is not at all clear that the cable adaptor 40 of Ozolins '858 reconstructs display information as recited, with respect to the receiver, in claim 1 and other independent claims of this application.

In the Office action, the Examiner also does not identify an element of Ozolins '858 corresponding to the synchronizing signal generator. However, Ozolins '858 (Figure 1) does disclose sync-stripper 60 which is described as extracting horizontal and vertical synchronization signals from either the green or composite signals (*see* column 3, lines 38-40 of the patent).

In the Office action, the Examiner does not identify an element corresponding to the digital-to-analog converter (DAC) recited as the third constituent element of the flat panel display apparatus recited in claim 1, and the fourth constituent element of the flat panel display apparatus recited in claim 2 of the present application.

Finally, in paragraph 3 of the Office action, the Examiner alleges that Ozolins '858 discloses "an output terminal for externally transferring synchronizing signal and analog video signal to an analog display" (quoting from paragraph 3, lines 4-5 of the Office action). However, the Examiner does not point out what element in Figure 1 of Ozolins '858 corresponds to the claimed output terminal. However, even if one presumes that the "output terminal" of Ozolins '858 consists of the various output lines extending from the right-hand portion of interface 20 (in Figure 1 of the patent)

toward the analog LCD panel 30, there is no disclosure or suggestion in Ozolins '858 of an output terminal connected to a synchronization signal generator and **to a DAC** for externally transferring the synchronizing signal and the analog video signal to an analog display apparatus.

The above comments relative to claim 1 apply equally to independent claim 2. Moreover, both dependent claim 11 (which is dependent from claim 1) and independent claim 2 further recite a video data converter for converting the video data so as to correspond to a prescribed display mode. In the Office action, the Examiner does not identify any element in Ozolins '858 corresponding to the claimed video data converter.

Dependent claims 15 and 34 recite that the flat panel display apparatus of the present invention operates without need for an analog-to-digital converter (ADC) or a phase-locked loop (PLL) circuit for signal conversion. In this regard, the Examiner states (in the sentence bridging pages 2 and 3 of the Office action) that "Ozolins teaches analog LCDs that are capable of utilizing analog RGB signals have [*sic*] been introduced to the market recently, although such analog LCDs do not require ADCs (see col. 1, lines 63-67 and col. 2, lines 1-6)" (quoting from the sentence bridging pages 2 and 3 of the Office action). However, the Examiner then concludes, from the latter statement, that "it would have been obvious to one of ordinary skill in the art at the time of invention to remove the phase-locked loop (90) as configured in Fig. 1" (quoting from page 2, lines 2-3 of the Office action). It is respectfully submitted that this constitutes a *non-sequitur* since the first statement of the Examiner does not lead logically to the conclusion contained in the second statement. In fact, even though Ozolins '858 appears to suggest that analog LCDs do not require

ADCs, when it comes to the inclusion of a PLL circuit in such a flat panel display terminal, Ozolins '858 positively teaches the inclusion of the PLL circuit 90 in the interface 20 shown in Figure 1 of the patent. Thus, Ozolins '858 **teaches away from** the concept of eliminating the PLL circuit 90 from such a flat panel display terminal. Therefore, one of ordinary skill in the art, upon reviewing Ozolins '858, would not be motivated to eliminate the PLL circuit 90, but rather would be motivated to **include** the PLL circuit 90 in such a flat panel display terminal. In short, Ozolins '858 teaches away from the concept of elimination of both ADCs and PLLs from a flat panel display apparatus, as taught by the present invention.

Dependent claims 5 and 23 recite the analog display apparatus as comprising the combination of an amplifier, a deflection signal generator, a high voltage generator, and a cathode ray tube (CRT). In paragraph 4 of the Office action, the Examiner admits that Ozolins '858 does not disclose a "deflection signal generator". However, the Examiner cites Rokunohe *et al.* '175 as disclosing an image transmission apparatus which includes a synchronizing signal generator 17, a deflection signal generator 62, a luminescent signal generator 63, and a video amplifier 64. The Examiner alleges that Rokunohe *et al.* '175 "is cited to show the concept of using a deflection signal generator (62) for receiving synchronizing signal output from synchronizing signal generator (17)" (quoting from paragraph 4, lines 7-9 of the Office action).

However, the deflection signal generator 62 of Rokunohe *et al.* '175 is included in Figure 8, and Figure 8 is a disclosure of the simulator 3 of Figure 6 (*see,* column 2, lines 67-68 of the patent). Figure 6, in turn, is a front view of a device producing an address converter to be used in the

arrangement of the patent, the address converter being shown as element 15 of Figure 2 (*see* column 2, lines 62-64 and Figures 2 and 6 of the patent). Thus, it is clear that, contrary to the recitations of the claims of this application, the deflection signal generator 62 of Rokunohe *et al.* '175 does not receive a synchronizing signal output, as alleged by the Examiner.

In paragraph 6 of the Office action, in connection with the rejection of claim 2, the Examiner admits that Ozolins '858 does not disclose a synchronizing signal generator as recited in claim 2. Therefore, the Examiner cites Sawada '317, and alleges that it teaches a display apparatus for displaying an image by receiving an RGB video signal which includes an image signal, and a display mode detector 15 which receives vertical and horizontal synchronizing signals.

In the latter regard, it should be noted that independent claim 1 also recites a synchronizing signal generator, but the Examiner, in rejecting claim 1, not only did not cite an element of Ozolins '858 corresponding to the claimed synchronizing signal generator, but also did not combine Ozolins '858 with Sawada '317 in rejecting claim 1.

At the top of page 5 of the Office action, the Examiner alleges that it would have been obvious to one of ordinary skill in the art to combine Ozolins '858 and Sawada '317 "to provide a display device which can perform display [of] an image in both the VGA and SVGA modes without using a PLL circuit for signal conversion" (quoting from page 5, lines 1-2 of the Office action). Whereas independent claims 1 and 2 no longer recite the limitation in question (*i.e.*, no need for any

analog-to-digital converter (ADC) and phase-locked loop (PLL) circuit for signal conversion), that limitation is now included in dependent claims 15 and 34. However, as mentioned above, Ozolins '858 actually **teaches away from** any elimination of a PLL circuit from the flat panel display apparatus since it **positively includes** the PLL circuit 90 in the interface 20 of the flat panel display apparatus 10 shown in Figure 1 of the patent. Thus, one of ordinary skill in the art, upon reviewing Ozolins '858, would not be motivated to eliminate the PLL circuit, but in fact, would be motivated to include the PLL circuit in any flat panel display apparatus.

Independent apparatus claim 9 and independent method claim 10 recite the invention in a manner distinguishable from the prior art for many of the same reasons discussed above relative to independent claims 1 and 2. That is, the Examiner has not cited any element in Ozolins '858 with regard to the means for or step of reconstructing display information. Furthermore, the prior art does not disclose or suggest conversion means which converts data to a corresponding video signal without utilization of a PLL circuit, as recited in claim 9, or a corresponding step as recited in method claim 10. In fact, as stated above, Ozolins '858 actually teaches away from the elimination of a PLL circuit by positively including a PLL circuit in the flat panel display apparatus shown in Figure 2 of the patent. For these reasons, independent apparatus claim 9 and independent method claim 10 recite the invention in a manner distinguishable from the prior art.

Finally, Applicant is submitting herewith a correction to a reference numeral contained in Figure 2 of the drawing. Figure 2 showing the correction in red, and a formal drawing of Figure 2 which incorporates the correction are attached.

In view of the above, it is submitted that the claims of this application are in condition for allowance, and early issuance thereof is solicited. Should any questions remain unresolved, the Examiner is requested to telephone Applicant's attorney.

A fee of $342.00 is incurred by the addition of nineteen (19) total claims in excess of total 20. Applicant's check drawn to the order of Commissioner accompanies this Amendment. Should the check become lost, be deficient in payment, or should other fees be incurred, the Commissioner is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,

Robert E. Bushnell,
Attorney for the Applicant
Registration No.: 27,774

1522 "K" Street N.W., Suite 300
Washington, D.C. 20005
(202) 408-9040

Folio: P55281
Date: 6/26/03
I.D.: REB/JGS